

## TITLE OF THE INVENTION

SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING  
THE SAME

## 5 BACKGROUND OF THE INVENTION

## Field of the Invention

The present invention relates to a semiconductor device, and more particularly to a CMOS transistor structure which provides for footprint savings.

## 10 Description of the Background Art

In employing a CMOS (Complementary Metal Oxide Semiconductor) transistor structure to form a semiconductor device, there is a need of connecting one of opposite  $N^+$ -type active regions of an n-channel MOS transistor and one of opposite  $P^+$ -type active regions of a p-channel MOS transistor, each of which is located in an outer  
15 portion of the CMOS transistor structure formed of the n-channel MOS transistor and the p-channel MOS transistor. Also, a wire connecting the  $N^+$ -type active region and the  $P^+$ -type active region should be disposed so as to be spatially separated from a gate electrode in order to avoid electrical connection between the wire and the gate electrode. Additionally, one example of a semiconductor device with a CMOS transistor structure is  
20 a CMOS inverter.

Another example is a nonvolatile semiconductor memory device as disclosed in Japanese Patent Application Laid-Open No. 2000-323590 (pages 9 through 12 and Figures 1 through 8), in which an interconnect layer buried in a self-aligned contact and a gate electrode are prevented from being short-circuited to each other.

25 While there has been no significant progress or change in a semiconductor

device with a CMOS transistor structure with respect to a function thereof, attempts have been made with respect to a configuration, to reduce a footprint of the CMOS transistor structure. However, in accordance with conventional practices, reduction of a footprint of a CMOS transistor structure in a semiconductor device has been subject to some constraints. One constraint is that a gate electrode and a wire connecting an N<sup>+</sup>-type active region and a P<sup>+</sup>-type active region should not overlap each other in plan view, in order to prevent the wire and the gate electrode from being electrically connected to each other. Another constraint is that a predetermined distance should be kept between the gate electrode and the wire connecting the N<sup>+</sup>-type active region and the P<sup>+</sup>-type active region, in order to allow for variations possibly caused during formation of the wire in manufacture of the device (an alignment error, for example).

#### SUMMARY OF THE INVENTION

It is an object of the present invention to provide a semiconductor device with a CMOS transistor structure, in which a gate electrode and a wire connecting an N<sup>+</sup>-type active region and a P<sup>+</sup>-type active region overlap each other in plan view, to reduce a footprint of the CMOS transistor structure.

According to a first aspect of the present invention, a semiconductor device with a CMOS transistor includes a plurality of gate electrodes, an n-channel MOS region, a p-channel MOS region and a wire. The plurality of gate electrodes are arranged in parallel with one another. The n-channel MOS region and the p-channel MOS region of the CMOS transistor are arranged adjacent to each other in a lengthwise direction of the plurality of gate electrodes. The wire connects the n-channel MOS region and the p-channel MOS region, and has a width greater than a distance between every two adjacent ones of the plurality of gate electrodes. Further, a portion of the wire is

disposed right above a portion of the gate electrode with an insulating film interposed therebetween.

The semiconductor device provides for reduction of a footprint of the CMOS transistor structure as compared to a conventional semiconductor device. Further, the distance between every two adjacent ones of the gate electrodes can be governed by a design rule without having to take into account the wire.

According to a second aspect of the present invention, a method of manufacturing a semiconductor device with a CMOS transistor includes a step of forming a gate electrode, a step of forming an insulating film, a step of forming an interlayer insulating film, a step of forming a first opening, a step of depositing a metal film and a step of removing a metal film. In the step of forming a gate electrode, a plurality of gate electrodes are formed so as to be arranged in parallel with one another on a semiconductor substrate. In the step of forming an insulating film, an insulating film is formed on a top face and a side face of the gate electrode. In the step of forming an interlayer insulating film, an interlayer insulating film made of a material different from a material for the insulating film, is formed on the insulating film. In the step of forming a first opening, etching is carried out on the interlayer insulating film using the insulating film as an etch stop layer, to form a first opening having a width greater than a distance between every two adjacent ones of the plurality of gate electrodes. In the step of depositing a metal film, a metal film is deposited on the interlayer insulating film. In the step of removing a metal film, the metal film on the interlayer insulating film, except a portion thereof which is buried in the first opening, is removed.

The method of manufacturing a semiconductor device provides for formation of a semiconductor device in which a self-aligned contact is formed and an insulating film serving as an etch stop layer is surely interposed between a wire and a gate electrode

which partly overlap each other in plan view.

These and other objects, features, aspects and advantages of the present invention will become more apparent from the following detailed description of the present invention when taken in conjunction with the accompanying drawings.

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#### BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1 is a plan view of a semiconductor device according to a first preferred embodiment of the present invention.

Fig. 2 is a sectional view of the semiconductor device according to the first  
10 preferred embodiment of the present invention.

Fig. 3 is a plan view of the semiconductor device according to the first preferred embodiment of the present invention.

Fig. 4 is a sectional view of the semiconductor device according to the first preferred embodiment of the present invention.

15 Fig. 5 is a plan view of the semiconductor device according to the first preferred embodiment of the present invention.

Fig. 6 is a sectional view of the semiconductor device according to the first preferred embodiment of the present invention.

Fig. 7 is a plan view of the semiconductor device according to the first  
20 preferred embodiment of the present invention.

Fig. 8 is a sectional view of the semiconductor device according to the first preferred embodiment of the present invention.

Fig. 9 is a plan view of the semiconductor device according to the first preferred embodiment of the present invention.

25 Fig. 10 is a sectional view of the semiconductor device according to the first

preferred embodiment of the present invention.

Fig. 11A is a plan view of the semiconductor device according to the first preferred embodiment of the present invention.

Fig. 11B is a plan view of a conventional semiconductor device.

5 Fig. 12 is a plan view of a semiconductor device according to a second preferred embodiment of the present invention.

Fig. 13 is a sectional view of the semiconductor device according to the second preferred embodiment of the present invention.

Fig. 14 is a plan view of an opening according to the second preferred  
10 embodiment of the present invention.

## DESCRIPTION OF THE PREFERRED EMBODIMENTS

### Preferred Embodiments

Below, the present invention will be described in detail, with reference to  
15 accompanying drawings which illustrate preferred embodiments of the present invention.

### First Preferred Embodiment

A semiconductor device with a CMOS transistor structure according to a first preferred embodiment will be described hereinafter by taking a CMOS inverter as a non-limiting example. Fig. 1 is a plan view of the semiconductor device according to  
20 the first preferred embodiment, at one stage during manufacture thereof. Fig. 2 is a sectional view of the semiconductor device according to the first preferred embodiment, at the same stage during manufacture thereof as in Fig. 1. In Fig. 1, an N<sup>+</sup>-type active region 1 of an n-channel MOS transistor and a P<sup>+</sup>-type active region 2 of a p-channel MOS transistor are formed in a surface portion of a semiconductor substrate by ion  
25 implantation or the like. Further, gate electrodes 3 each used in both the n-channel

MOS transistor and the p-channel MOS transistor are formed on the  $N^+$ -type active region 1 and the  $P^+$ -type active region 2 by photolithography. The semiconductor device according to the first preferred embodiment can be regarded as including an n-channel MOS region where the n-channel MOS transistor is formed and a p-channel  
 5 MOS region where the p-channel MOS transistor is formed.

The gate electrodes 3 are arranged orthogonally to the  $N^+$ -type active region 1 and the  $P^+$ -type active region 2. Further, insulating films 4 made of silicon nitride are deposited on the gate electrodes 3 by CVD (Chemical Vapor Deposition) or the like, as illustrated in Fig. 2. Fig. 2 is a sectional view taken along a line II-II in Fig. 1, which  
 10 illustrates the gate electrodes 3 and the insulating films 4 sequentially deposited on the semiconductor substrate. A distance between every two adjacent ones of the gate electrodes 3 may be governed by a design rule (i.e., a minimum distance which can be achieved by photolithography used in manufacture).

Fig. 3 is a plan view of the semiconductor device according to the first  
 15 preferred embodiment, at one stage during manufacture thereof. Fig. 4 is a sectional view of the semiconductor device according to the first preferred embodiment, at the same stage during manufacture thereof as in Fig. 3. As illustrated in Fig. 3, an insulating film 5 made of silicon nitride is formed on each of side faces of the gate electrodes 3 by CVD or the like. The insulating film 5 may be called a sidewall. Fig.  
 20 4 is a sectional view taken along a line IV-IV in Fig. 3. As illustrated in Fig. 4, each of the gate electrodes 3 is covered with the insulating films 4 and 5 with no portion thereof being exposed.

Fig. 5 is a plan view of the semiconductor device according to the first preferred embodiment, at one stage during manufacture thereof. Fig. 6 is a sectional  
 25 view of the semiconductor device according to the first preferred embodiment, at the

same stage during manufacture thereof as in Fig. 5. As illustrated in Fig. 5, an interlayer insulating film 6 made of silicon oxide is formed over the gate electrodes 3 covered with the insulating films 4 and 5, by CVD or the like. Fig. 6 is a sectional view taken along a line VI-VI in Fig. 5. As illustrated in Fig. 6, the interlayer insulating film 6 is planarized by CMP or the like in order to achieve a uniform distance from a top face of the interlayer insulating film 6 to the insulating films 4, as a preparation to make openings which are to be formed for accommodating wires connecting the  $N^+$ -type active region 1 and the  $P^+$ -type active region 2, uniform in size.

Fig. 7 is a plan view of the semiconductor device according to the first preferred embodiment, at one stage during manufacture thereof. Fig. 8 is a sectional view of the semiconductor device according to the first preferred embodiment, at the same stage during manufacture thereof as in Fig. 7. As illustrated in Fig. 7, openings 7 for accommodating the wires connecting the  $N^+$ -type active region 1 and the  $P^+$ -type active region 2 are formed in the interlayer insulating film 6. Each of the openings 7, the greatest width of which is greater than the distance between every two adjacent ones of the gate electrodes 3, has a two-part structure formed of an upper opening and a lower opening. Each of the upper openings is formed by etching a portion of the interlayer insulating film 6 to a depth at which the top face of one of the insulating films 4 which serves as an etch stop layer exists. This etching process is carried out under process condition which allows a high etch selectivity of an oxide film relative to a nitride film by an order of magnitude or more.

Each of the lower openings is formed by etching a portion of the interlayer insulating film 6 using the insulating films 5 as an etch stop layer, to expose a portion of a top face of each of the  $N^+$ -type active region 1 and the  $P^+$ -type active region 2. In view of the fact that the insulating films 4 and 5 are used as an etch stop layer in forming

the openings 7, each of the openings 7 is a self-aligned contact. This ensures that the insulating films 4 and 5 are interposed between each of wires to be buried in the openings 7 and each of the gate electrodes 3 which partly overlap each other in plan view. Accordingly, it is possible to prevent the wires buried in the openings 7 and the gate electrodes 3 from being electrically connected to each other.

Fig. 8 is a sectional view taken along a line VIII-VIII in Fig. 7. As illustrated in Fig. 8, a metal film such as an aluminum film is buried in the openings 7. More specifically, a metal film is deposited in the openings 7 and on the interlayer insulating film 6 by sputtering or the like, and then CMP or the like is carried out to remove each portion of the metal film which is not buried in the openings 7, thereby to planarize the metal film. As a result, wires 8 (hereinafter, referred to as "buried wires 8") connecting the  $N^+$ -type active region 1 and the  $P^+$ -type active region 2 are formed as illustrated in Figs. 9 and 10. Fig. 9 is a plan view of the semiconductor device according to the first preferred embodiment. Fig. 10 is a sectional view of the semiconductor device according to the first preferred embodiment, taken along a line X-X in Fig. 9. The greatest width of each of the buried wires 8 is greater than the distance between every two adjacent ones of the gate electrodes 3. The buried wires 8 are located in part thereof right above portions of the gate electrodes 3 with the insulating films 4 interposed therebetween. It is additionally noted that a technique used for planarizing the metal film is not limited to CMP. Alternatively, etch back can be used, in which the metal film is anisotropically etched so that only a projecting portion of the metal film can be selectively removed.

Fig. 11A is a plan view of an example of the semiconductor device (CMOS inverter) according to the first preferred embodiment. In the example of Fig. 11A, a 0.2- $\mu$ m design rule is employed, so that the distance between every two adjacent ones of



the gate electrodes 3 is  $0.2\ \mu\text{m}$ . Accordingly, a footprint of a CMOS transistor structure in this example of the CMOS inverter which is indicated by a broken line in Fig. 11A is  $1.2\ \mu\text{m} \times (0.1\ \mu\text{m} + 0.2\ \mu\text{m} + 0.1\ \mu\text{m}) = 0.48\ \mu\text{m}^2$ .

For the purpose of comparison, one example of a conventional CMOS inverter is shown in Fig. 11B. As shown in Fig. 11B, the conventional CMOS inverter is configured such that the buried wires 8 and the gate electrodes 3 do not overlap one another in plan view. In the example of Fig. 11B, a  $0.2\text{-}\mu\text{m}$  design rule is employed and a margin of  $0.15\ \mu\text{m}$  is left during manufacture in order to avoid overlap between the buried wires 8 and the gate electrodes 3. Accordingly, a footprint of a CMOS transistor structure in this example of the conventional CMOS inverter which is indicated by a broken line in Fig. 11B is  $1.2\ \mu\text{m} \times (0.13\ \mu\text{m} + 0.15\ \mu\text{m} + 0.2\ \mu\text{m} + 0.15\ \mu\text{m} + 0.13\ \mu\text{m}) = 0.91\ \mu\text{m}^2$ . As is appreciated from comparison between the examples shown in Figs. 11A and 11B, the CMOS inverter having the structure according to the first preferred embodiment (in a typical case where a gate electrode of the CMOS inverter has a width (W) of approximately  $1\ \mu\text{m}$ ) provides for reduction of a footprint of the CMOS transistor structure by about 50% relative to the conventional CMOS inverter.

As described above, the semiconductor device with a CMOS transistor structure according to the first preferred embodiment, includes the gate electrodes 3 and the buried wires 8 connecting the n-channel MOS region and the p-channel MOS region. The semiconductor device is configured such that the greatest width of each of the buried wires 8 is greater than the distance between every two adjacent ones of the gate electrodes 3, and the buried wires 8 are located in part thereof right above portions of the gate electrodes 3 with the insulating films 4 interposed therebetween. This provides for reduction of a footprint of the CMOS transistor structure in the entire device, as compared to the conventional semiconductor device. Also, it is possible to govern the

distance between every two adjacent ones of the gate electrodes 3 by a design rule without having to take into account the buried wires 8.

Further, in the semiconductor device according to the first preferred embodiment, the insulating films 4 and 5 are formed on the top faces and the side faces of the gate electrodes 3, and then the buried wires 8 are buried in the openings 7 which are formed by carrying out etching on the interlayer insulating film 6 using the insulating films 4 and 5 as an etch stop layer. Thus, the openings 7 are self-aligned contacts. This ensures that the insulating films 4 and 5 serving as an etch stop layer are interposed between each of the buried wires 8 and each of the gate electrodes 3 which partly overlap each other in plan view. Moreover, a method of manufacturing a semiconductor device according to the first preferred embodiment, as described above, provides for formation of the semiconductor device in which self-aligned contacts are formed and the insulating films 4 and 5 serving as an etch stop layer are surely interposed between each of the buried wires 8 and each of the gate electrodes 3 which partly overlap each other in plan view.

Furthermore, in the method of manufacturing a semiconductor device according to the first preferred embodiment, the buried wires 8 may be formed by carrying out etch back on a metal film deposited on the interlayer insulating film 6 in which the openings 7 have been formed. This simplifies a process, as compared to a method which includes CMP for treating the metal film.

#### Second Preferred Embodiment

Also a semiconductor device with a CMOS transistor structure according to a second preferred embodiment will be described by taking a CMOS inverter as a non-limiting example. Fig. 12 is a plan view of the semiconductor device according to

the second preferred embodiment. In an analogous manner to the first preferred embodiment, according to the second preferred embodiment, the CMOS inverter includes the  $N^+$ -type active region 1 of the n-channel MOS transistor and the  $P^+$ -type active region 2 of the p-channel MOS transistor which are formed in a surface portion of a semiconductor substrate by ion implantation or the like. Further, the gate electrodes 3 each used in both the n-channel MOS transistor and the p-channel MOS transistor are formed on the  $N^+$ -type active region 1 and the  $P^+$ -type active region 2 by photolithography.

The gate electrodes 3 are arranged orthogonally to the  $N^+$ -type active region 1 and the  $P^+$ -type active region 2. Moreover, the insulating films 4 and 5 made of silicon nitride are formed on the gate electrodes 3. The interlayer insulating film 6 made of silicon oxide is formed over the gate electrodes 3 covered with the insulating films 4 and 5, by CVD or the like. It is noted that illustration of the interlayer insulating film 6 is omitted in Fig. 12. Then, the openings 7 for accommodating the wires connecting the  $N^+$ -type active region 1 and the  $P^+$ -type active region 2 are formed in the interlayer insulating film 6. Each of the openings 7, the greatest width of which is greater than a distance between every two adjacent ones of the gate electrodes 3, has a two-part structure formed of an upper opening and a lower opening.

Each of the upper openings of the openings 7 is formed by etching a portion of the interlayer insulating film 6 to a depth at which a top face of one of the insulating films 4 which serves as an etch stop layer exists. This etching process is carried out under process condition which allows a high etch selectivity of an oxide film relative to a nitride film by an order of magnitude or more. Each of the lower openings of the openings 7 is formed by etching a portion of the interlayer insulating film 6 using the insulating films 5 as an etch stop layer, to expose a portion of a top face of each of the  $N^+$

-type active region 1 and the P<sup>+</sup>-type active region 2. In view of the fact that the insulating films 4 and 5 are used as an etch stop layer in forming the openings 7, each of the openings 7 is a self-aligned contact.

According to the second preferred embodiment, openings 9 are additionally  
 5 formed on the gate electrodes 3 so that portions of the gate electrodes 3 are exposed. Each of the openings 9 is formed by etching respective predetermined portions of one of the insulating films 4 and one of the insulating films 5, by photolithography. Then, a metal film such as an aluminum film is buried in the openings 7 and 9. More specifically, a metal film is deposited in the openings 7 and 9 and the interlayer insulating  
 10 film 6 by sputtering or the like, and then CMP or the like is carried out to remove each portion of the metal film which is not buried in the openings 7 and 9, thereby to planarize the metal film. As a result, the buried wires 8 are formed. The greatest width of each of the buried wires 8 is greater than the distance between every two adjacent ones of the gate electrodes 3. The buried wires 8 are located in part thereof right above portions of  
 15 the gate electrodes 3 with the insulating films 4 interposed therebetween.

Fig. 13 is a sectional view of the semiconductor device according to the second preferred embodiment. Fig. 13 is a sectional view taken along a line XIII-XIII in Fig. 12. Fig. 13 illustrates a state where respective portions of one of the insulating films 4 and one of the insulating films 5 have been removed as a result of forming the opening 9  
 20 so that one of the buried wires 8 is electrically connected to one of the gate electrodes 3. Additionally, also in the second preferred embodiment, a technique used for planarizing the metal film for forming the buried wires 8 is not limited to CMP. Alternatively, etch back can be carried out on the metal film deposited on the interlayer insulating film 6 having the openings 7 and 9 formed therein, to form the buried wires 8. To employ etch  
 25 back would simplify a process, as compared to a case where CMP is employed for

treating the metal film.

Each of the openings 7 and each of the openings 9 are provided so as to form one continuous opening which provides not a rectangular shape, but a shape having six corners or more, in the interlayer insulating film 6 in plan view. Fig. 14 is a plan view of the opening formed of one of the openings 7 and one of the openings 9. The opening which provides a shape having six corners or more in plan view allows electrical connection to be established at more portions in the device than an opening which is simply rectangular in plan view. This increases flexibility in layout of the semiconductor device.

As described above, in the semiconductor device according to the second preferred embodiment, the buried wires 8 are further provided in the openings 9 which are formed by removing portions of the insulating films 4 and 5, to be electrically connected to the gate electrodes 3. This makes it possible to obtain a configuration which allows the buried wires 8 to be connected to the gate electrodes 3, as well as to reduce a footprint of the CMOS transistor structure as compared to the conventional device. Also, a method of manufacturing a semiconductor device according to the second preferred embodiment, as described above, provides for formation of a semiconductor device in which a footprint of a CMOS transistor structure included therein is reduced as compared to the conventional semiconductor device and the buried wires 8 can be connected to the gate electrodes 3.

Further, in the semiconductor device according to the second preferred embodiment, each of the openings 7 and each of the openings 9 form one continuous opening which provides a shape having six corner or more in the interlayer insulating film 6 in plan view. This makes it possible to establish electrical connection between regions located not in line with each other, thereby to increase flexibility in layout of the

semiconductor device.

While the invention has been shown and described in detail, the foregoing description is in all aspects illustrative and not restrictive. It is therefore understood that numerous modifications and variations can be devised without departing from the scope  
5 of the invention.